MICROELECTRONIC CIRCUITS

ADEL S. SEDRA
Department of Electrical Engineering
University of Toronto

KENNETH C. SMITH
Department of Electrical Engineering and Computer Science
University of Toronto

Holt, Rinehart and Winston

New York Chicago San Francisco Philadelphia
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Mexico City Rio de Janeiro Madrid

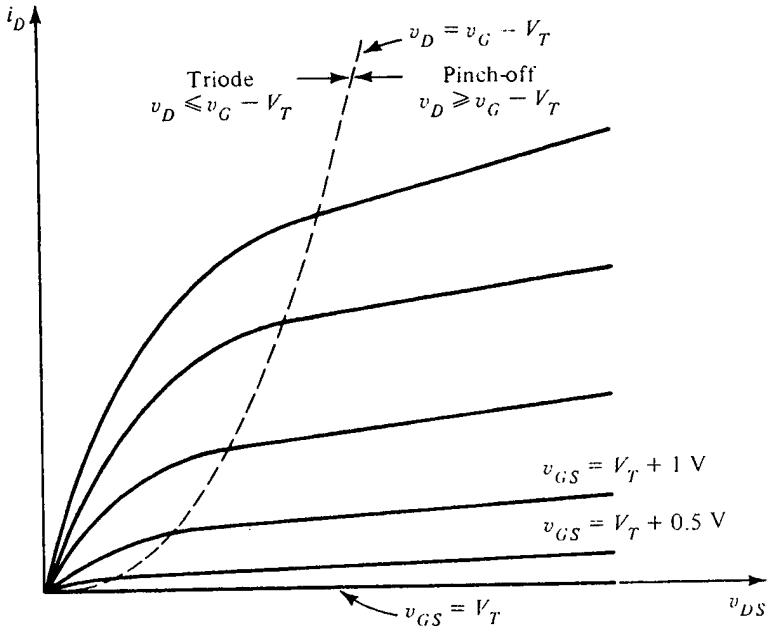

Fig. 8.15 Actual characteristics of n-channel MOSFET, illustrating the finite nonzero slope in the pinch-off region. Note that the slope increases with the current level in the device. Thus the output resistance r_o is inversely proportional to the bias current I_D.

In the following we shall study two popular biasing arrangements for enhancement MOSFETs.

A First Biasing Scheme

Figure 8.16 shows our first biasing arrangement; although it looks identical to that used for biasing JFETs and depletion-type MOSFETs, the principle of operation is some-

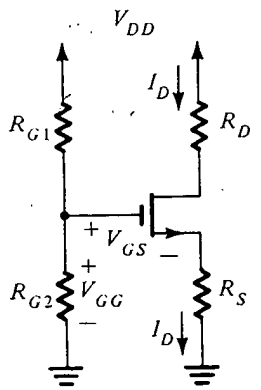

Fig. 8.16 A popular biasing arrangement for enhancement MOS amplifiers.

head on the source points in the direction of normal current flow. Finally, note that the symbol for the *p*-channel device is drawn with the source up, which makes it conform with our circuit-drawing convention of currents flowing from top to bottom.

Recapitulation

Consider Fig. 8.14. For the *n*-channel enhancement device shown in the figure to conduct, v_{GS} has to be positive and greater than V_T. The device will operate in the pinch-off or active region if the drain voltage v_D is more positive than the gate voltage v_G by

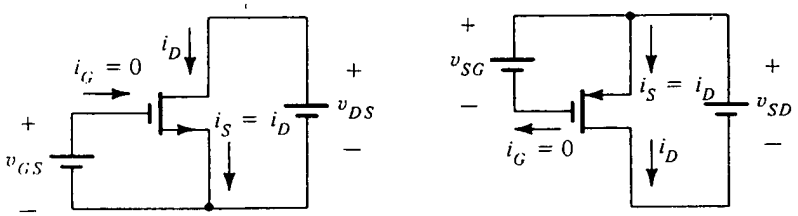

Fig. 8.14 Normal current flow directions and voltage polarities in enhancement MOS transistors.

at least $-V_T$. That is, the device will still be in pinch-off even if the drain voltage is lower than that of the gate by V_T volts. If the drain voltage is further reduced, the device gets out of pinch-off and goes into the triode region.

For the *p*-channel device to conduct, the source has to be made more positive than the gate by at least $|V_T|$ volts; that is, $v_{SG} \geq |V_T|$. The device will be in pinch-off as long as the drain voltage is lower than that of the gate, or even if it is higher than that of the gate by at most $|V_T|$. If v_D is increased more than $|V_T|$ volts above v_G, the device leaves pinch-off and enters the triode region.

Of course, the pinch-off region is the one suitable for amplifier application. Switching applications make use of the cutoff region and the triode region.

Finally, we should point out that real devices display a finite output resistance when operated in the pinch-off region. Figure 8.15 shows the i_D-v_{DS} characteristics of an *n*-channel MOS transistor of the enhancement type. In pinch-off the characteristic curves show finite slope that increases with the current level in the device.

EXERCISE

8.2 Consider an enhancement NMOS transistor with $V_T = 2$ V which conducts a current $i_D = 1$ mA when $v_{GS} = v_{DS} = 3$ V. What is the value of i_D for $v_{GS} = 4$ V and $v_{DS} = 5$ V? (Assume that in pinch-off the device acts as a current source.) Also calculate the value of the drain-to-source resistance r_{DS} for small v_{DS} and $v_{GS} = 4$ V.
Ans. 4 mA; 500 Ω

8.3 BIASING THE ENHANCEMENT MOSFET

As mentioned before, the first step in the design of a transistor amplifier involves establishing a stable and predictable dc operating point inside the active region of operation.